74ABT16244A

16-bit buffer/line driver; 3-state

Rev. 05 — 10 February 2006 Product data sheet

1. General description

The 74ABT16244A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16244A is a 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs (1$\overline{OE}$, 2$\overline{OE}$, 3$\overline{OE}$, 4$\overline{OE}$), each controlling four of the 3-state outputs.

2. Features

- 16-bit bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +64 mA and –32 mA
- Live insertion and extraction permitted
- Latch-up performance: JESD 78 Class II
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - CDM JESD 22-C101-C exceeds 1000 V

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay from nAx to nYx	C_L = 50 pF; V_{CC} = 5 V	1.1	1.7	2.6	ns
t_{PHL}	propagation delay from nAx to nYx	C_L = 50 pF; V_{CC} = 5 V	1.3	2.1	2.9	ns
C_{in}	input capacitance	V_I = 0 V or V_{CC}	-	4	-	pF
C_o	output capacitance	V_O = 0 V or V_{CC}; outputs disabled	-	7	-	pF
I_{CC}	quiescent supply current	V_{CC} = 5.5 V				
		outputs disabled	-	0.45	1.0	mA
		outputs LOW	-	10	19	mA

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4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16244ADGG	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ABT16244ADL	–40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

5. Functional diagram

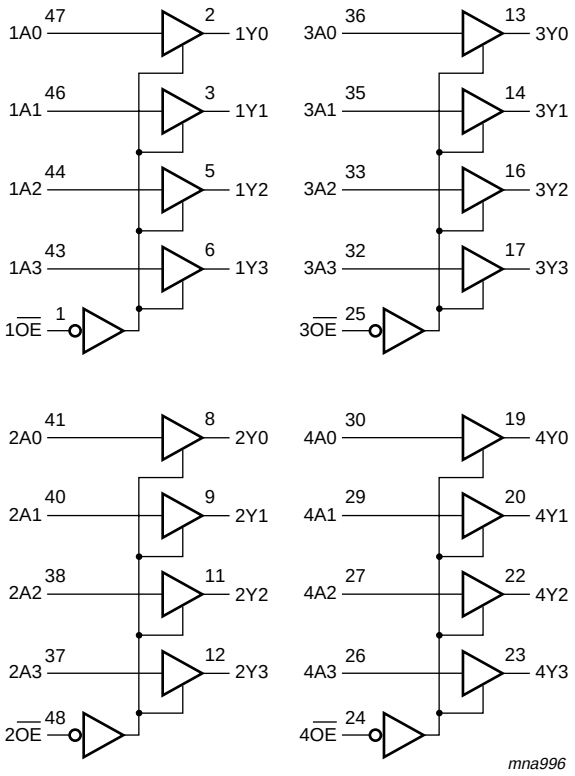


Fig 1. Logic symbol

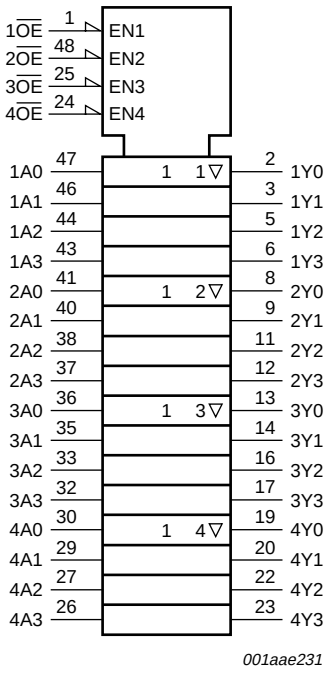


Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

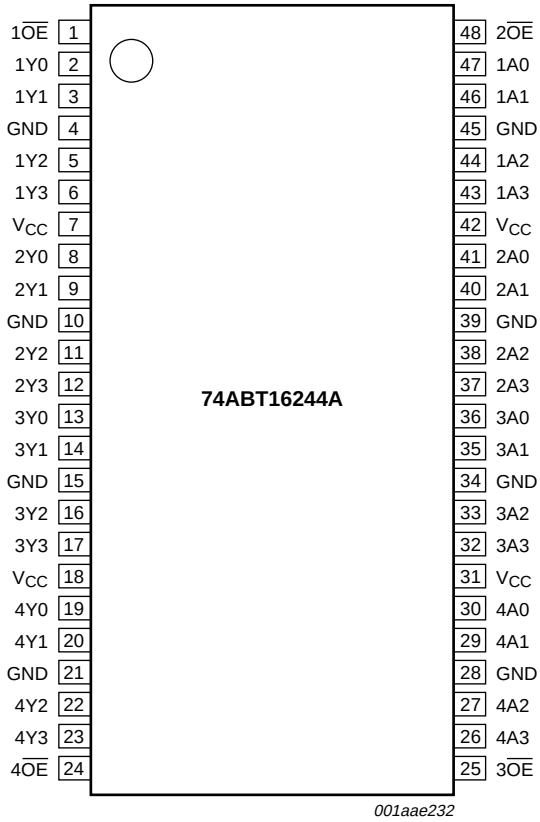


Fig 3. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	1 output enable (LOW active)
1Y0	2	1 data output 0
1Y1	3	1 data output 1
GND	4	ground (0 V)
1Y2	5	1 data output 2
1Y3	6	1 data output 3
V_{CC}	7	supply voltage
2Y0	8	2 data output 0
2Y1	9	2 data output 1
GND	10	ground (0 V)
2Y2	11	2 data output 2

Table 3. Pin description *…continued*

Symbol	Pin	Description
2Y3	12	2 data output 3
3Y0	13	3 data output 0
3Y1	14	3 data output 1
GND	15	ground (0 V)
3Y2	16	3 data output 2
3Y3	17	3 data output 3
V_{CC}	18	supply voltage
4Y0	19	4 data output 0
4Y1	20	4 data output 1
GND	21	ground (0 V)
4Y2	22	4 data output 2
4Y3	23	4 data output 3
$4\overline{OE}$	24	4 output enable (LOW active)
$3\overline{OE}$	25	3 output enable (LOW active)
4A3	26	4 data input 3
4A2	27	4 data input 2
GND	28	ground (0 V)
4A1	29	4 data input 1
4A0	30	4 data input 0
V_{CC}	31	supply voltage
3A3	32	3 data input 3
3A2	33	3 data input 2
GND	34	ground (0 V)
3A1	35	3 data input 1
3A0	36	3 data input 0
2A3	37	2 data input 3
2A2	38	2 data input 2
GND	39	ground (0 V)
2A1	40	2 data input 1
2A0	41	2 data input 0
V_{CC}	42	supply voltage
1A3	43	1 data input 3
1A2	44	1 data input 2
GND	45	ground (0 V)
1A1	46	1 data input 1
1A0	47	1 data input 0
$2\overline{OE}$	48	output enable 2 (LOW active)

7. Functional description

7.1 Function table

Table 4. Function table[1]

Control	Input	Output
$n\overline{OE}$	nAx	nYx
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don t care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–18	mA
V_I	input voltage		[1]	–1.2	+7.0	V
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_j	junction temperature		[2]		150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
I_{OH}	HIGH-state output current		-	-	–32	mA

Table 6. Recommended operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OL}	LOW-state output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	–0.9	–1.2	V
V_{OH}	HIGH-state output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	2.9	-	V
		I_{OH} = –32 mA		2.0	2.4	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	3.4	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}; I_{OL} = 64 mA		-	0.42	0.55	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	±0.01	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_O or V_I ≤ 4.5 V		-	±5.0	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = V_{CC}	[1]	-	±5.0	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		outputs HIGH-state at V_O = 5.5 V		-	0.1	10	µA
		outputs LOW-state at V_O = 0.0 V		-	–0.1	–10	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	–100	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}	[3]				
		outputs HIGH-state		-	0.45	1.0	mA
		outputs LOW-state		-	10	19	mA
		outputs disabled		-	0.45	1.0	mA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[1][3]				
		outputs enabled, one data input		-	100	250	µA
		outputs disabled, one data input		-	100	250	µA
		per input pin; V_{CC} = 5.5 V; one enable input at 3.4 V; other inputs at V_{CC} or GND		-	100	250	µA
C_{in}	input capacitance	V_I = 0 V or V_{CC}		-	4	-	pF
C_o	output capacitance	V_O = 0 V or V_{CC}; outputs disabled		-	7	-	pF
T_{amb} = –40 °C to +85 °C							
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		-	-	–1.2	V

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OH}	HIGH-state output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		2.5	-	-	V
		I_{OH} = –32 mA		2.0	-	-	V
		V_{CC} = 5.0 V; V_I = V_{IL} or V_{IH}					
		I_{OH} = –3 mA		3.0	-	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 4.5 V; V_I = V_{IL} or V_{IH}; I_{OL} = 64 mA		-	-	0.55	V
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V		-	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0.0 V; V_O or V_I ≤ 4.5 V		-	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = V_{CC}	[1]	-	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}					
		outputs HIGH-state at V_O = 5.5 V		-	-	10	µA
		outputs LOW-state at V_O = 0.0 V		-	-	–10	µA
I_{CEX}	output HIGH-state leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}		-	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–50	-	–180	mA
I_{CC}	quiescent supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}	[3]				
		outputs HIGH-state		-	-	1.0	mA
		outputs LOW-state		-	-	19	mA
		outputs 3-state		-	-	1.0	mA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[1][3]				
		outputs enabled, one data input		-	-	250	µA
		outputs disabled, one data input		-	-	250	µA
		per input pin; V_{CC} = 5.5 V; one enable input at 3.4 V; other inputs at V_{CC} or GND		-	-	250	µA

[1] This is the increase in supply current for each input at 3.4 V.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed 1 s.

[3] This data sheet limit may vary among suppliers.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

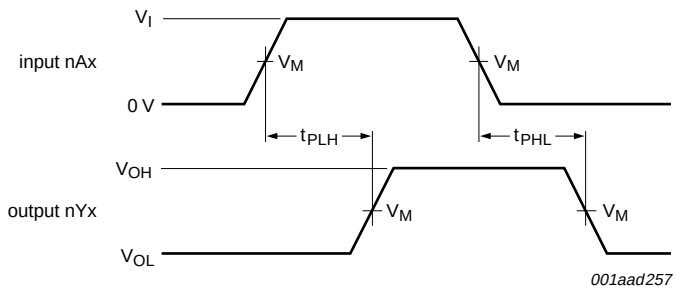
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C; V_{CC} = 5.0 V						
t_{PLH}	propagation delay from nAx to nYx	see Figure 4	1.1	1.7	2.6	ns
t_{PHL}	propagation delay from nAx to nYx	see Figure 4	1.3	2.1	2.9	ns
t_{PZH}	output enable time to HIGH-state	see Figure 5	1.6	2.7	3.7	ns
t_{PZL}	output enable time to LOW-state	see Figure 5	2.3	3.5	4.0	ns
t_{PHZ}	output disable time from HIGH-state	see Figure 5	1.5	3.0	4.0	ns

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLZ}	output disable time from LOW-state	see Figure 5	1.6	2.4	3.2	ns
T_{amb} = −40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V						
t_{PLH}	propagation delay from nAx to nYx	see Figure 4	1.1	-	2.8	ns
t_{PHL}	propagation delay from nAx to nYx	see Figure 4	1.3	-	3.4	ns
t_{PZH}	output enable time to HIGH-state	see Figure 5	1.6	-	4.5	ns
t_{PZL}	output enable time to LOW-state	see Figure 5	2.3	-	4.8	ns
t_{PHZ}	output disable time from HIGH-state	see Figure 5	1.5	-	4.6	ns
t_{PLZ}	output disable time from LOW-state	see Figure 5	1.6	-	4.1	ns

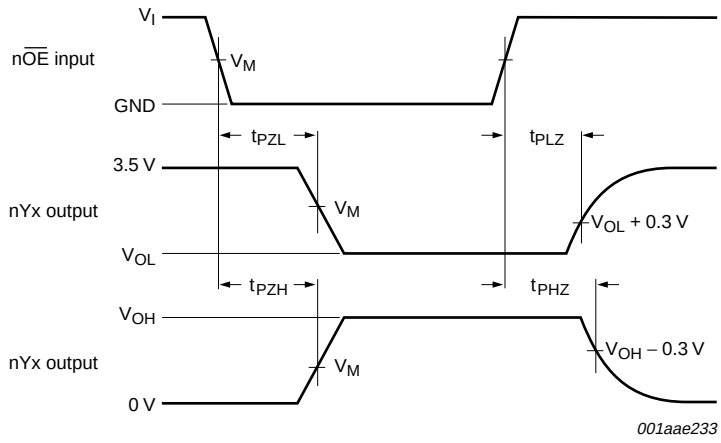
12. Waveforms



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

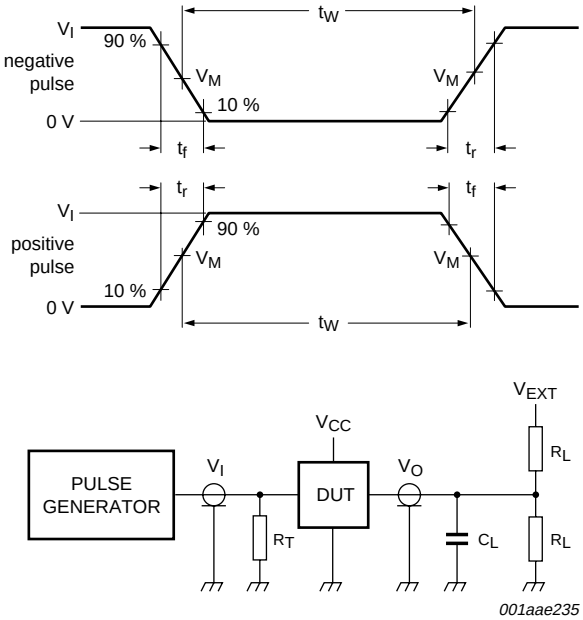
Fig 4. Input (nAx) to output (nYx) propagation delay



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. 3-state output enable and disable times



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

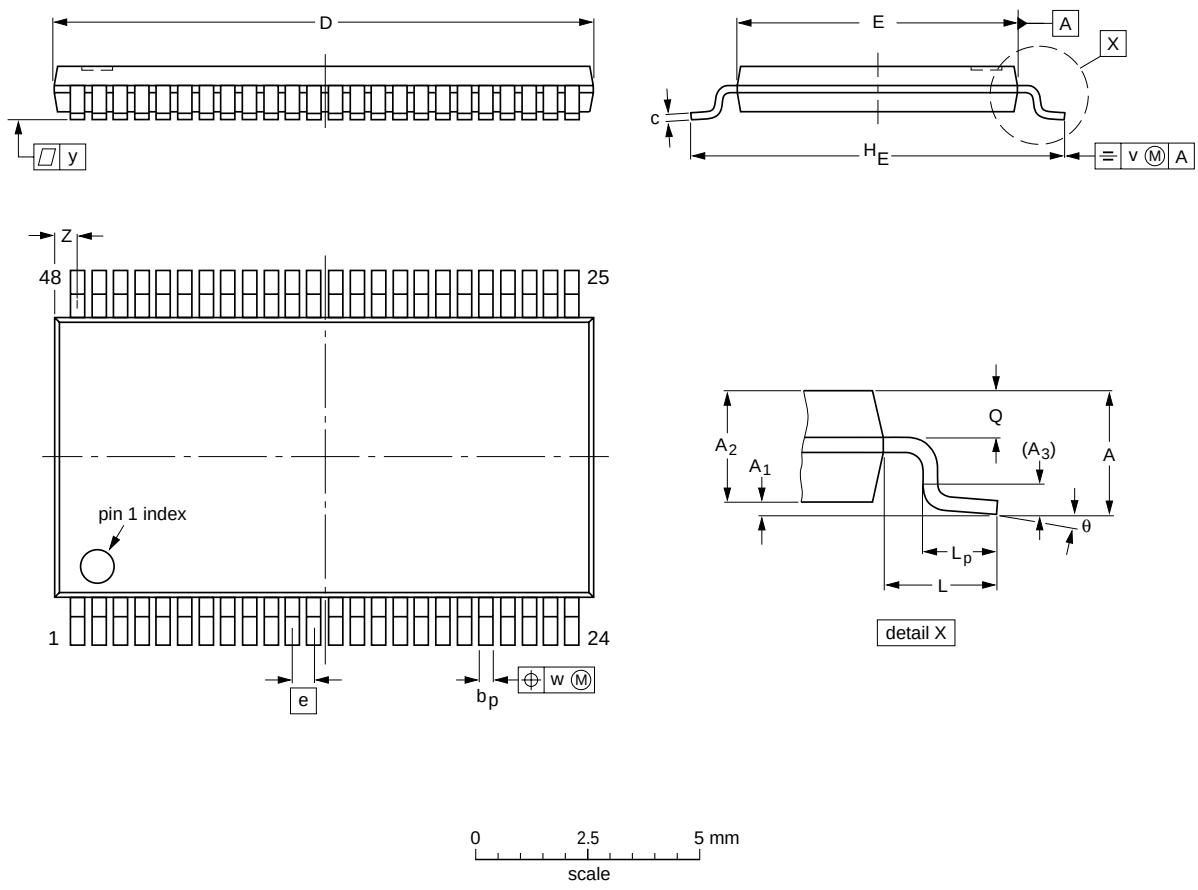
Fig 6. Load circuitry for switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

13. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

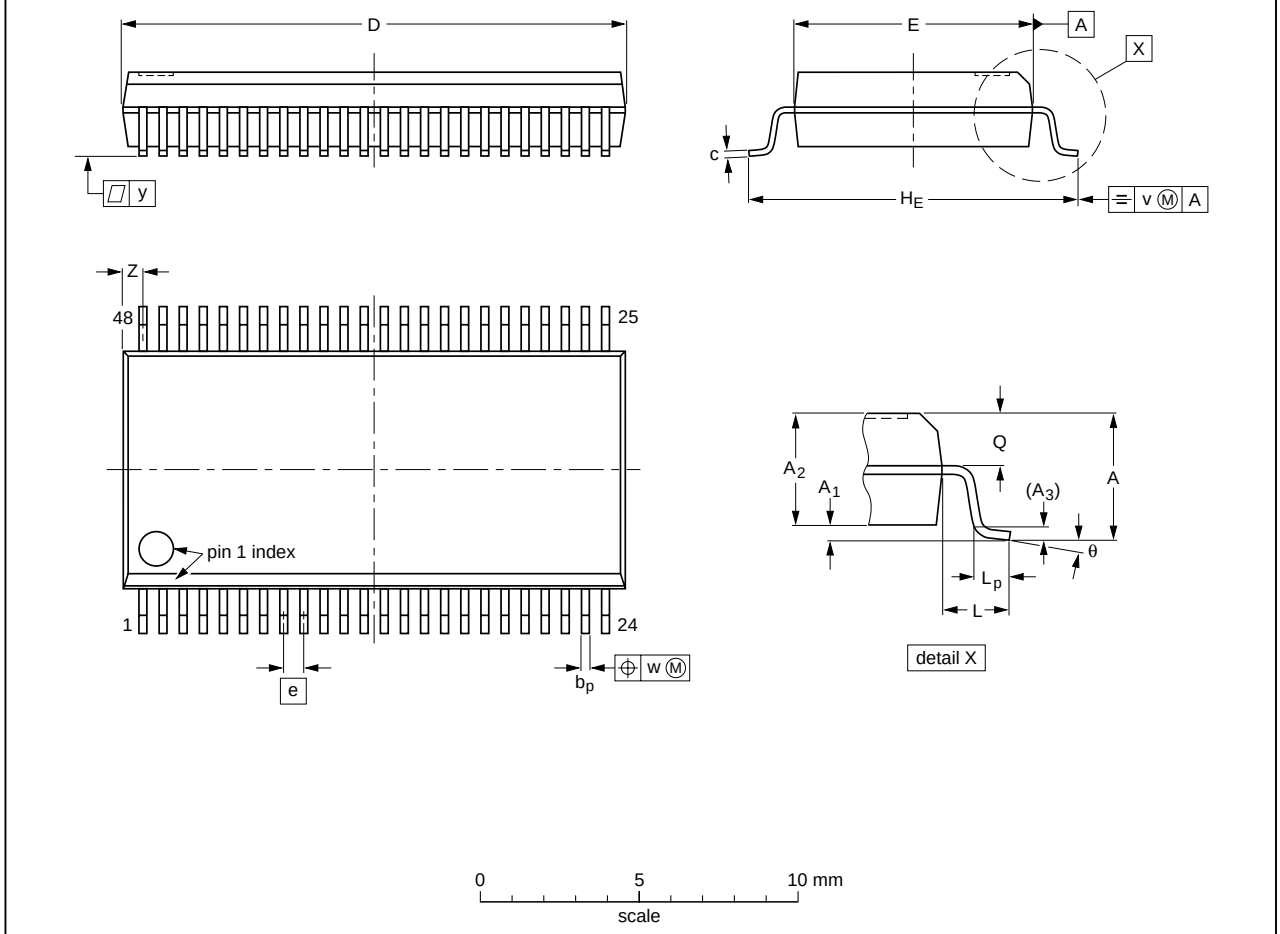
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT362-1 (TSSOP48)

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT370-1 (SSOP48)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16244A_5	20060210	Product data sheet	-	74ABT_H16244A_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Removed all information of the 74ABTH16244A product • Section 2 “Features”: changed latch-up feature to JESD 78 and added ESD protection feature • Section 11 “Dynamic characteristics”: changed t_{PHZ} minimum values from 2.0 ns to 1.5 ns			
74ABT_H16244A_4 (9397 750 04709)	19981007	Product specification	-	74ABT_H16244A_3
74ABT_H16244A_3 (9397 750 03484)	19980225	Product specification	-	74ABT_H16244A_2

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 10 February 2006

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